

Introduction

The following information is a direct result of a significant amount of time spent in response to questions from users of Intersil analog switches. Among the variety of questions are a few which seem to be asked more frequently than others. Over the next few pages, these questions are discussed with the hope that the answers will be helpful to the users and potential users of Intersil analog switches. Some questions are technical in nature while others are simply questions on interpretation of the Intersil Analog Data Book.

Power Supply Considerations

The first two questions are similar questions and the explanation will apply to both:

1. If the power supplies are off, will the switch be open? (Present a high impedance to the input signal)
2. If the power supplies are off, can an input signal be applied?

Both of these questions refer to an overvoltage condition when the supplies are off and an input signal is applied. A common misunderstanding is that the switch will be open and block the signal when actually the opposite occurs.

What is meant by the power supplies being off? Does it refer to the supplies being shorted to ground or does it imply they are open circuited?

If the power supplies go to ground, the input signal will pass through the switch and appear at the output. The explanation for this can be seen in Figure 1, which is a simplified CMOS switch cell. This switch cell consists of two enhancement type field effect transistors, one N-channel and one P-channel. An enhancement type of device is a FET which is normally off without some potential (gate voltage) to turn it on. A P-channel FET requires a negative potential (gate to source voltage) to turn it on and an N-channel FET requires a positive potential (gate to source). Contained in the physical structure of the FETs are parasitic transistors which are shown in Figure 1 as diodes from the source and drain to the body potentials of the devices. These diodes or parasitic junctions are normally reversed biased. If those junctions are forward biased, a fault condition exists where the signal is passed through the parasitic transistor. This is what occurs if the power supplies go to ground. Depending on the polarity of the input signal, either the N or P channel FET parasitics will be forward biased and the signal passed through the switch.

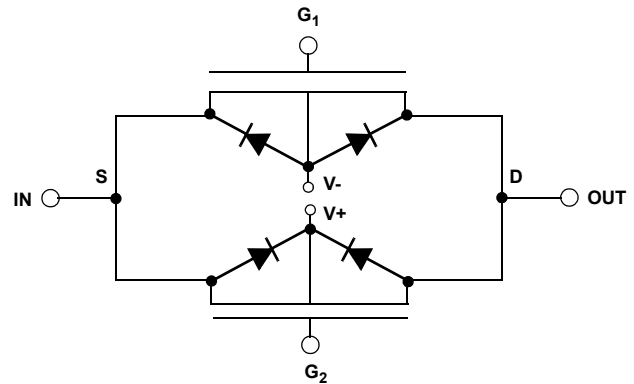


FIGURE 1. BASIC CMOS TRANSMISSION GATE

Having the signal pass through the switch may be acceptable in some applications, but most likely it is not. An example would be a user who was switching various voltages (transducers) as shown in Figure 2. If the supplies go to ground and these signals pass through the switch, the input voltage sources could easily be shorted.

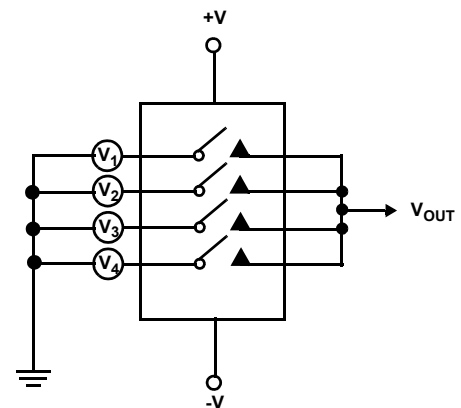


FIGURE 2. SWITCHING MULTIPLE INPUTS

Another situation occurs if the power supplies are open circuited where the most positive and negative input signals will provide power to the switch. In this case, the signals being used for power will be passed to the output, but the remaining switches with inputs less than those used for supply will operate properly.

Input Overvoltage Protection

There is a possibility that the switch will be damaged if exposed to excessive current levels during an overvoltage condition. A second overvoltage condition is the case where the input signals exceed the existing power supply levels. Neither of these situations are recommended and the following questions are similar to those frequently asked.

3. Can an input greater than the supplies be applied?
4. In my application, there is a possibility that the switch will lose power and the input signal will still be applied. Is there a way to protect the switch if this situation occurs?

Referring to Figure 1 once again, if the input signal exceeds the supply by an amount greater than the breakdown voltage of the parasitic junction, the normally reversed biased junction will come forward biased. These forward biased junctions will pass the input signals to the output and possibly short out the voltage sources.

The most common form of protection circuit for these types of overvoltage conditions is the resistor-diode network at the input of the switch as shown in Figure 3.

This circuit protects the device if the supplies go to ground or if the input exceeds the supply. If either of these situations occur, the diodes will be forward biased and current path to ground will exist. This will protect the switch from excessive current levels. The primary purpose of the resistor is to limit the current through the diode.

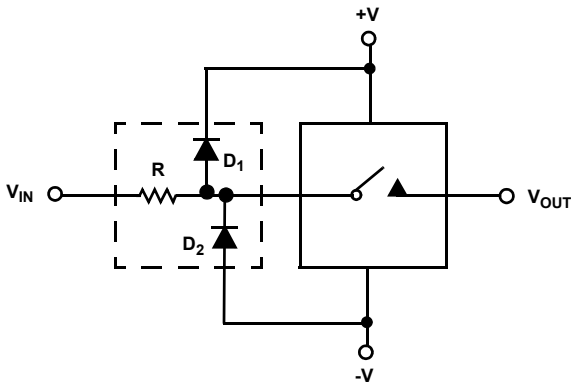


FIGURE 3. PROTECTION FOR EACH ANALOG INPUT

Another advantage of using diode protection is that it prevents the input signal from passing to the output. This is a result of the input being clamped to the breakdown voltage of the protection diodes. If this breakdown voltage is less than the threshold voltage (turn on voltage) of the parasitic diodes, the parasitic transistor will remain reverse biased and the signal will not pass through the switch.

There are some disadvantages to the user with this type of protection. One would be the economics involved with using external protection for each analog input. This could present a cost problem if a large number of channels were involved. Another concern would be the current limiting resistors

which adds to the on resistance of the switch contributing to the overall system error. A further possible source of error is current leakage in the diodes. It is recommended that low leakage diodes, such as schottky diodes be used.

The protection circuit just discussed is not used to protect the switch from latch up. The Intersil switches are constructed using the dielectric isolation process and the four layer SCR found in JI technology does not exist. This circuit is intended to protect the device from high current levels which result from the forward biasing of the parasitic transistors which are inherent in all FET structures.

If for some reason the resistor-diode protection circuit cannot be used, there are other possibilities. The following method may help to avoid the extra cost of protecting each input. In this method, since the supplies are open circuited, the most positive and most negative signal will power-up the chip and any input with signals less than those being used for power will operate properly. However, this method can only be used if the outputs are not common and a user can afford to have at least two signals pass to the output.

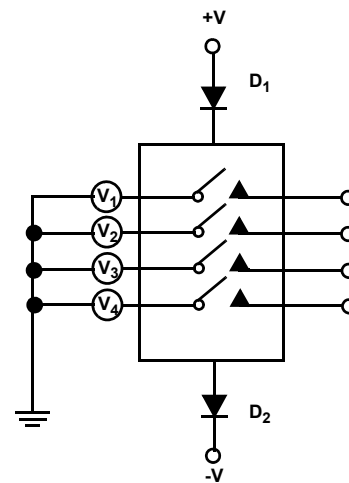


FIGURE 4. POWERING THE SWITCH WITH THE INPUT SIGNALS

Another alternative does not involve protection circuitry, but instead takes advantage of CMOS technology. An example would be a user who has $\pm 15V$ supplies and needs to switch a $+18V$ signal as shown in Figure 5. This appears to be an overvoltage condition since the input exceeds the supply. But rather than protect the device, the user can shift the supplies to $+20V, -10V$. Now the input signal is within the supply level and the switch should work properly. In certain applications the supply voltages can be adjusted in order to pass a larger range of input signals.

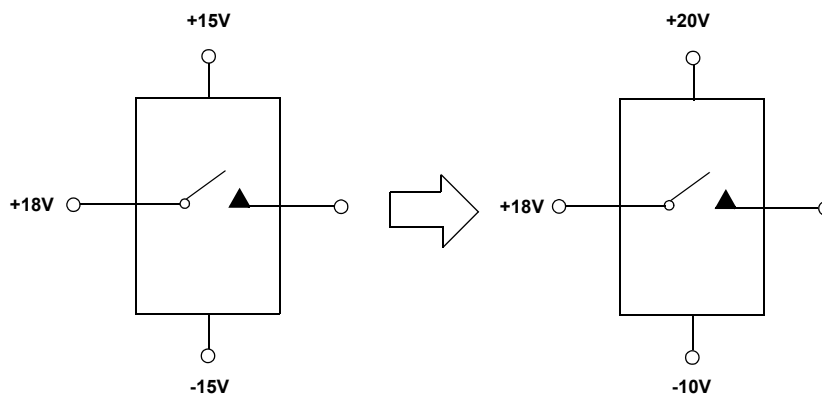


FIGURE 5. VARYING THE SUPPLIES TO MEET THE $V_{IN} < V$ SUPPLY REQUIREMENTS

Single Supply Operation

Single supply operation is a topic which is discussed frequently and the following are examples of typical questions.

5. Can the switch be operated at a single power supply?
6. What is the minimum power supply possible?

Usually engineers with critical power requirements request a single supply operation. An example would be battery operated applications such as portable equipment. In these cases the designer is limited to single supply, low supply or both.

Trade-offs exist with single supply operation that should be pointed out to the user. An example is the HI-300 series of switches which has the capability of operating with a single +5V supply. The performance of the switch will vary, however, as supply voltage decreases, the on resistance and the switching times increase. A 300 series switch with a single +5V supply will have higher on resistance and slower switching speeds than the same device at $\pm 15V$ or even a single +15V supply. This represents a change in both DC and AC performance. Even though the switch may now meet the user's power requirements at single supply, the question is whether it will still meet the performance requirements.

The explanation for these variations can be found in the FET devices composing the switch cell itself. The variation in on resistance is due to the fact that the channel impedance of FET is dependent on the gate-source bias. Since the gate voltage is determined by the supply voltage, it can be concluded that the on resistance is a function of the supply voltage.

The fact that the on resistance varies with supply voltage directly relates to the slower switching times, since the higher on resistance will reduce the available current needed to charge the internal capacitance of the switch. Lower changing current relates directly to slower switching times.

Questions about Intersil Switches

Many of the questions asked about switches could apply to any CMOS switch manufacturer's products. But some questions are unique to both the Intersil product line and data catalog. The following are examples of some of the more common questions concerning the Intersil Analog Data Catalog.

7. What is the difference between the V_L and V_R pins on the HI-5043 and V_{REF} pins on the HI-201?

The device pins mentioned above have their own individual functions even though they are all associated with the logic reference circuits of their respective designs. For the HI-201, the V_{REF} pin is the terminal which establishes the logic threshold levels for which the switch will change state. Although it is normally left open when driving from +5V logic (DTL or TTL), it can be connected to a higher supply in order to raise the switching threshold levels when driving CMOS Logic greater than 5V. The V_{REF} pin enables the user to change from TTL to CMOS Logic.

The reference circuit of the HI-50XX series of switches is different from the HI-201, which accounts for the V_R and V_L pins. Even though the V_R terminal is brought out on the package, it is recommended that this pin be grounded. This terminal determines the ground for the internal reference circuit. The V_L pin performs a similar function to the V_{REF} pin on the HI-201. It is normally connected to 5V for TTL Logic but can be tied to a higher supply for CMOS levels. This effectively raises the switching thresholds to accommodate the higher CMOS level.

The next question is easily the most frequently asked question about Intersil HI-50XX series of switches.

8. Are the switch functions shown on the data sheet a result of the logic address being HIGH or LOW?

Actually, the answer to the question is printed at the top of the data sheet page, depicting switch functions "switch states are for a logic 1 input". Therefore, the address is in the HIGH state for the switch functions shown on that page.

Some other areas which are often questioned on the data sheets are the minimum ratings and performance between channels of the switches. The following questions are typical:

9. Will the switch operate at the absolute maximum ratings?

The topic of absolute maximum ratings does create some confusion. Basically, the contents of the Electrical characteristic table are the guaranteed parameters. The switch may operate with conditions other than those recommended, but are not guaranteed parameters. Anything above absolute maximum ratings may permanently damage the device.

Problems sometimes arise when a customer tests some parts at conditions other than those which are guaranteed. If the parts work, the user may go ahead and design around those conditions. But there is a good possibility the next batch of switches may not perform in the same manner. The user must be aware that anything outside the guaranteed limits is a user's risk and susceptible to variations in manufacturing.

10. What is the variation in "on" resistance between channels on the switch?

There are two cause for these variations. One cause is process variation, which is due to variables in manufacturing. This can create variation between channels on the same unit. The second reason is lot variation which can cause differences in performance from unit to unit. After all variations are taken into account, a good "rule of thumb" is $\pm 10\%$ tolerance on typical parameter values. So if a device has a typical on resistance of 50Ω , a user could expect a $\pm 5\Omega$ variation.